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EXAMINER	
TRAN, KHUONG N	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,170	BACK, DAE-WHAN	
	Examiner	Art Unit	
	Khuong Tran	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: On page 5, line 4 the third multiplexer is labeled with a wrong part number. It should be **110** instead of **170**.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Mok (US Patent No. 5,440,571).

Regarding claim 1, Mok teaches an addressing circuit that makes use of a memory buffer for controlling the addressing function. The teaching entails a buffer memory **[200, figure 3]** for storing symbol data for the logical channel **[figure 2]** according to input sequence so that the symbol data are stored in a continuous arrangement **[column 3, lines 51-60]**. Subsequently, Mok mentions the storing of start addresses by using D flip-flops as the start address table for storing address information according to the logical channels **[figure 2]** where

each address information indicates a location of initial symbol data stored in the buffer memory **[column 4 lines 16-20, figure 5C]**. Furthermore, the control signal generating circuit **[100, figure 4]** consists of multiplexers **[2, 5, 8, figure 4]** where MUX3 outputs the address according to the enable signal SEL2 coming from the controller unit 11 set for each logical channel **[figure 2]**.

Regarding claim 2, Mok discloses in figure 2 of the drawings where symbol data are stored continuously. The total number of data produced in one frame of a tape is 1456 words **[column 2, lines 14-16]**. The data symbols are stored in both channel A and channel B. Therefore, when the storage of symbols for one channel has been completed, an initial symbol of another logical channel is subsequently stored a position of a word in the buffer memory next to the already stored symbol as shown in **figure 2**.

Regarding claim 3, Mok illustrates in figure 4 the address output is produced by the third multiplexer MUX3 **[8, figure 4]**. Signals must be processed sequentially by other components in the circuit prior to reaching the third multiplexer. For instance, the address table, which Mok replaces by D flip-flops **[7, figure 4]**, is used for storing the address information. Before the address information is outputted to the Q terminal of the flip-flop, the clock CLK2 (pulse signal as shown in **figure 5A**) must be at the enable state before the address information from the table can be inputted to MUX3. Since the enable state from the CLK2 signal is one of the inputs going to the D flip-flop, it is part of the address table.

Regarding claim 6, Mok discloses a way to managing addresses using a buffer memory in an addressing circuit. The technique involves storing symbol data according to the logical channels **[figure 2]** according to the input sequences in the buffer memory so the data between logical channels are stored in a continuous arrangement **[column 3, lines 51-60]**. The step further includes storing the address information according to the logical channels in a start address table, each of the address information indicating a location of the initial symbol data corresponding to the logical channels **[column 4, lines 12-20]**. It is noted in figure 2 that the channels illustrate the allocation of data symbols of the main region in one frame **[column 2, lines 61-63]**. Additionally, the addressing circuit also has multiplexers **[2, 5, 8, figure 4]** for selectively outputting the address information stored in the address table by an enable select signal SEL2 **[figure 4]** set for each logical channel **[column 4, lines 28-40]**.

Regarding claim 7, Mok discloses in figure 2 of the drawings where symbol data are stored continuously. The total number of data produced in one frame of a tape is 1456 words **[column 2, lines 14-16]**. The data symbols are stored in both channel A and channel B. Therefore, when the storage of symbols for one channel has been completed, an initial symbol of another logical channel is subsequently stored a position of a word in the buffer memory next to the already stored symbol as shown in **figure 2**.

Regarding claim 8, Mok illustrates in figure 4 the address output is produced by the third multiplexer MUX3 **[8, figure 4]**. Signals must be processed sequentially by other components in the circuit prior to reaching the third

multiplexer. For instance, the address table, which Mok replaces by D flip-flops **[7, figure 4]**, is used for storing the address information. Before the address information is outputted to the Q terminal of the flip-flop, the clock CLK2 (pulse signal as shown in **figure 5A**) must be at the enable state before the address information from the table can be inputted to MUX3. Since the enable state from the CLK2 signal is one of the inputs going to the D flip-flop, it is part of the address table.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 5, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mok (US Patent No. 5,440,571) in view of Witkowski et al (US Patent No. 6,201,789).

Regarding claims 4 and 9, Mok teaches the use of a memory buffer to support the storage of data symbols from logical channels as applied to claims 1 and 6. The teaching further explains that data symbols are stored in the buffer in a continuous manner from address 0 in the memory buffer **[column 3, lines 51-60]**. Figure 2 also entails the data symbols storing across channels in an

arrangement that when one channel is complete, the next symbol will be stored in the next channel next to the already stored symbol **[figure 2]**. Mok however does not teach any mechanism to log the linking of data across different storage sectors in the memory buffer for the case of data that expand over one sector. Witkowski et al teaches a network switch consists of a memory device having a data packet portion and a hash portion, where the data packet portion comprises a plurality of sectors of data packets chained together using link addresses. According to one preferred embodiment in the teaching, the sectors are initially linked into a freepool chain of sectors. As data packets are received, a receive sector chain is created for each port by pulling sectors from the freepool chain as needed **[column 3, lines 54-62]**. As a result, the link addresses enable the data packets stored in different sectors to be transmitted and received in their entirety. Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the teaching of Mok to include link addresses in the memory buffer to handle data symbols that are stored in more than one sector as taught by Witkowski et al. One is motivated as such for including transmit address links to form a transmit packet chain for each port receiving data packets for transmission **[column 3, lines 62-65]**. Hence making the network switch useful for facilitating communication in a network system with a plurality of networks coupled to the switch ports **[column 3, lines 15-17]**.

Regarding claims 5 and 10, Mok teaches the use of D flip-flops to support the indexing of data symbols from the buffer memory by storing the start addresses of each data frame as applied to claims 1 and 6. The teaching further

explains that data symbols are stored in the buffer in a continuous manner from address 0 in the memory buffer **[column 3, lines 51-60]**. Figure 2 also entails the data symbols storing across channels in an arrangement that when one channel is complete, the next symbol will be stored in the next channel next to the already stored symbol **[figure 2]**. Mok however does not teach any mechanism to log the linking of data across different storage sectors in the starting address table for the case of data that expand over one sector. Witkowski et al teaches a network switch consists of a memory device having a data packet portion and a hash portion, where the data packet portion comprises a plurality of sectors of data packets chained together using link addresses. According to one preferred embodiment in the teaching, the sectors are initially linked into a freepool chain of sectors. As data packets are received, a receive sector chain is created for each port by pulling sectors from the freepool chain as needed **[column 3, lines 54-62]**. As a result, the link addresses enable the data packets stored in different sectors to be transmitted and received in their entirety. Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the teaching of Mok to include link addresses in the start address tables, which comprise of D flip-flops, to handle data symbols that are stored in more than one sector as taught by Witkowski et al. One is motivated as such for including transmit address links to form a transmit packet chain for each port receiving data packets for transmission **[column 3, lines 62-65]**. Hence making the network switch useful for facilitating communication in a

network system with a plurality of networks coupled to the switch ports **[column 3, lines 15-17]**.

Conclusion

6. Any response to this Office Action should be **faxed** to (571) 273-8300 or **mailed** to:

Commissioner for Patents,
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khuong Tran, whose telephone number is (571) 270-3522. The examiner can normally be reached Mon-Fri from 7:30AM - 5:00PM.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Q. Tieu, can be reached at (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information

for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have question on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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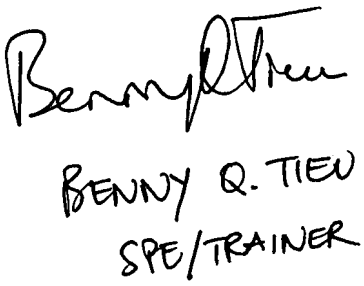
September 13, 2007



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